\$	DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD	AAAAAAA AAAAAAA AAAAAAA	
SSS SSS SSS SSS SSS	DDD DDD	AAA AAA	
\$\$\$ \$\$\$	DDD DDD	AAA AAA	
555555555	DDD DDD DDD DDD	AAA AAA	
\$\$\$\$\$\$\$\$\$ \$\$\$\$\$\$\$\$\$	DDD DDD	AAA AAA	
SSS	DDD DDD	AAAAAAAAAAAA	
\$\$\$ \$\$\$ \$\$\$	DDD DDD DDD DDD	AAA AAA	
SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS	DDD DDDDDDDDDD DDD	AAA AAA	
\$	DDDDDDDDDDDDDDDDD	AAA AAA	

VV	AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA	XX	000000 00 00 00 00	PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	\$
RRRRRRRR RRRRRRRR RR RR RR RR RR RR RR RR RRRRRR		QQQQQQ QQ QQ QQ QQ			

**

Version:

'V04-000'

VAXOPS.REQ - OP CODE TABLE FOR VAX INSTRUCTIONS

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Author:

KEVIN PAMMETT, MARCH 2, 1977.

Modified by:

V001

TMH0001 Tim Halvorsen 09-Feb-1981
Rewrite macro invocations to supply the entire SRM operand specification, to allow checking for literals in write operands, and other invalid conditions.

LITERAL

OPERAND ACCESS TYPE (A,B,M,R,V,W) - 1 BIT WIDE

ACCESS_A = 0, ACCESS_B = 0, ACCESS_R = 1, ACCESS_W = 0, ACCESS_W = 0, ACCESS_V = 0, EFFECTIVE ADDRESS
BRANCH DISPLACEMENT
OPERAND IS READ-ONLY
OPERAND IS WRITE-ONLY
OPERAND IS MODIFIED
ADDRESS A SET OF 2 REGISTERS

OPERAND DATA TYPE (B,W,L,Q,F,D,G,H,V) - 3 BITS WIDE

DATA_B = 0,

! BYTE CONTEXT

```
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VAXOPS.REQ:1
              DATA_W = 1,

DATA_L = 2,

DATA_Q = 3,

DATA_F = DATA_L,

DATA_D = DATA_Q,

DATA_G = DATA_Q,

DATA_H = 4,
                                                                                WORD CONTEXT
LONGWORD CONTEXT
QUADWORD CONTEXT
                                                                                FLOATING CONTEXT
FLOATING DOUBLE CONTEXT (8 BYTES)
FLOATING GRAND CONTEXT (8 BYTES)
FLOATING HUGE CONTEXT (16 BYTES)
   BRANCH DISPLACEMENT TYPES
               NO_BRANCH = 0,
BRANCH_BYTE = 1,
BRANCH_WORD = 2;
                                                                                NO BRANCH
                                                                                BRANCH BYTE
                                                                                BRANCH WORD
  THE FOLLOWING MACRO IS USED TO BUILD SUCCESSIVE ENTRIES FOR THE TABLE. EACH MACRO CALL CONTAINS THE INFO FOR 1 VAX OPCODE, AND THE ENTRIES ARE SIMPLY BUILT IN THE ORDER THAT THE MACRO CALLS ARE MADE - THE ASSUMPTION IS THAT THEY WILL BE MADE IN ORDER OF INCREASING OPCODE VALUES. THIS IS NECESSARY BECAUSE THE TABLE IS ACCESSED BY USING A GIVEN OPCODE AS THE
   TABLE INDEX.
COMPILETIME $BRANCH_TYPE=0;
MACRO
      GET_1ST(A,B) = AX,
GET_2ND(A,B) * BX,
OPERAND(NAME) *
               XIF XNULL (MAME)
               *THEN
               XELSE
                      BEGIN
XIF NOT XDECLARED (XSTRING ('ACCESS_', GET_1ST (XEXPLODE (NAME))))
                              %WARN('invalid access type ',GET_%ST(%EXPLODE(NAME)))
                       XIF NOT XDECLARED (XSTRING ('DATA_', GET_2ND (XEXPLODE (NAME))))
                       XTHEN
                              XWARN('Invalid data type ',GET_2ND(%EXPLODE(NAME)))
                       XIF NAME EQL 'BB'
                       XTHEN.
                       XASSIGN($BRAMCH_TYPE, BRANCH_BYTE)
XELSE XIF NAME EQL 'BW'
XTHEN
                               %ASSIGN($BRANCH_TYPE, BRANCH_WORD)
                      %FI %FI
%NAME('DATA_',GET_2ND(%EXPLODE(NAME))) +
%NAME('ACCESS_',GET_1ST(%EXPLODE(NAME))) ^ 3
```

..........

```
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 VAXOPS.REQ:1
              XFI X.
       OPDEF(NAME, OPC, OP1, OP2, OP3, OP4, OP5, OP6) = XASSIGN($BRANCH_TYPE, NO_BRANCH)
              %RAD50_11 NAME.

%IF GET_1ST(%EXPLODE(NAME)) EQL 'X'

AND GET_2ND(%EXPLODE(NAME)) EQL 'X'

! Opcode name in RAD50
! If undefined opcode,
               %THEN
                      NOT_AN_OP
                                                                                     ! then no operands
               %ELSE
                      %LENGTH-2
                                                                                     ! else, number of operands
               %FI OR
                     OPERAND (OP1) 4.
                                                                                     ! Define each operand
              OPERAND (OP2) OR
                     OPERAND (OP3) 4.
              OPERAND (OP4) OR
                     OPERAND (OP5) 4.
              OPERAND (OP6) OR
                     $BRANCH_TYPE^4%;
                                                                             ! Define branch context
   MACROS TO ACCESS THE FIELDS.
MACRO
      OP_NAME = 0.0.32.0%, ! OPCODE MNEUMONIC (6 RAD50 CHARS)
OP_NUMOPS = 4.0.4.0%, ! NUMBER OF OPERANDS
OP_CONTEXT(I) = 4+1/2, ((I) AND 1)*4, 3, 0 %, ! OPERAND CONTEXT
OP_DATATYPE(I) = 4+1/2, ((I) AND 1)*4 + 3, 1, 0 %, ! OPERAND DATA TYPE
OP_BR_TYPE = 7,4,4,0 %; ! CONTEXT OF BRANCH DISPLACEMENT
LITERAL
             OPTSIZE = 8,
MAXOPCODE = "XX'FD",
                                                            EACH OPINFO BLOCK IS 9 BYTES LONG.
MAXIMUM VAX OP CODE WHICH IS VALID.
MAXIMUM NUMBER OF OPERANDS PER INSTRUCTION.
              MAXOPRNDS = 6,
                                                            NO INSTRUCTION THAT HAS BRANCH TYPE ADDRESSING CAN HAVE THIS MANY OPERANDS UNLESS WE CHANGE THE ORGANIZATION OF EACH OPINFO BLOCK.

NUMBER OF BITS IN A VAX BYTE.

NUMBER OF PROCESSOR REGISTER, 'AP'.

NUMBER OF PROCESSOR REGISTER, 'PC'.
              BITS PER BYTE = 8,
AP_REG = 12,
PC_REG = 15,
              PC_REL_MODE = 8,
AT_PC_REL_MODE = 9,
INDEXING_MODE = 4,
                                                            ADDRESSING MODE: (PC)+
                                                            ADDRESSING MODE: a(PC)+
                                                         ! ADDRESSING MODE: XXX[RX]
              SHORT_LIT_AMODE = 0,

REGISTER_AMODE = 5,

REG_DEF_AMODE = 6,

AUTO_DEC_AMODE = 7,

AUTO_INC_AMODE = 8,

DISP_BYTE_AMODE = 10,
                                                            Short literals fit right into the mode byte.
                                                            Register mode addressing.
                                                            Register deferred addressing mode.
Auto decrement addressing mode.
                                                             Auto Increment addressing mode.
                                                            All of the displacement modes start from
                                                            here. See ENC_OPERAND() IN DBGENC.B32
              DISP_LONG_AMODE = 14,
OP_CR_SIZE = 6;
                                                         ! SIZE, IN ASCII CHARS, OF OPCODE MNEMONIC.
```

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VAXOPS.REQ:1
MACRO
            DSPL_MODE = 0,4,4,0 %,
                                                      ADDRESSING MODE BITS FROM THE DOMINANT MODE
                                                        BYTE OF AN OPERAND REFERENCE.
            DOM_MOD_FIELD = 0,5,2,1 %
                                                      BITS WHICH WE PICK UP TO DIFFERENTIATE CERTAIN TYPES OF DOMINANT MODES. SEE DBGMAC.B32
             SHORT_LITERAL = 0,0,6,0
                                                     HOW TO EXCTRACT A 'SHORT LITERAL' FROM
THE INSTRUCTION STREAM. SEE SRM.
BITS OF DOMINANT MODE ADDRESSING BYTE
WHICH SPECIFY THE ACTUAL MODE.
BITS OF DOMINANT MODE ADDRESSING BYTE
WHICH SPECIFY REGISTER NUMBER, ETC.
OP NUMOPS INDICATOR FOR UNASSIGNED OPCODES.
             AMODE
                         = 0,4,4,1 %,
             AREG
                         = 0,0,4,0 %,
            NOT_AN_OP = 15 %
             RESERVED = 'UNUSED' %:
                                                      NAME OF RESERVED OPCODES.
MACRO
            NEXT_FIELD(INDEX)
                                                      USED TO GET THE ADDRESS OF THE NEXT
                                                         FIELD OF A BLOCK.
                         = (INDEX), 0, 0, 0, 0%;
    MACROS AND LITERALS SPECIFICALLY FOR INSTRUCTON ENCODING.
    ('MACHINE -IN'.)
LITERAL
            BAD_OPCODE
BAD_OPERAND
BAD_OPRNDS
INS_RESERVED
                                      = 1.
                                                      CAN'T INTERPRET THE GIVEN ASCII OPCODE.
                                                      UNDECODABLE OPERAND REFERENCE.
                                                     WRONG NUMBER OF OPERANDS.
GIVEN OPCODE IS RESERVED.
                                      = 4:
LITERAL
                         ! We only have to special-case a few OPCODES,
            OP_CASEB
OP_CASEW
OP_CASEL
                                      = %X'8F'.
                                      = %X'CF':
1++
            TOKEN VALUES USED FOR ENCODING/DECODING
!--
LITERAL
            indexing_token = 240.
            byte_val_token = val_token + %SIZE(VECTOR[1,BYTE]),
word_val_token = val_token + %SIZE(VECTOR[1,WORD]),
brch_token = 244,
long_val_token = val_token + %SIZE(VECTOR[1,LONG]),
at_reg_token = 246,
register_token = 247,
lit_token = 248,
bad_token = 249;
                                                                                                      ! 245
```

MA

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 VAXOPS.REQ:1
 ! The following structure declaration selects the proper opcode ! table by looking for the extended opcode opcode(s).
STRUCTURE OPCODE_TBL [OPC,O,P,S,E] =

BEGIN

EXTERNAL LIB$GB_OPINFO1 : BLOCKVECTOR[256,OPTSIZE,BYTE];

EXTERNAL LIB$GB_OPINFO2 : BLOCKVECTOR[256,OPTSIZE,BYTE];

LOCAL OFFSET;

OFFSET = 0;

IF (OPC AND %X'FF') NEQ %X'FD'

THEN LIB$GB_OPINFO1[OPC,OFFSET,0,8,0] ! One byte opcodes

ELSE LIB$GB_OPINFO2[(OPC^-8),OFFSET,0,8,0] ! Two byte opcodes

END<P,S,E>;
                                                                                                                                                                                                                                                                                                                                                                     L1
                     VAXOPS.REQ
                                                         - last line
```

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